REMARKS

In the Office Action dated August 12, 2002, claims 20-22 were objected to; claims 1-22 were rejected under 35 U.S.C. § 102 over U.S. Patent No. 6,076,139 (Welker); and claim 23 was rejected under § 103(a) over Welker.

OBJECTIONS TO CLAIMS 20-22

Claims 20-22 have been amended to address the objection.

REJECTIONS UNDER 35 U.S.C. §§ 102 AND 103:

As amended, claim 1 is allowable over Welker. The Office Action pointed to the collection of the multi-channel memory interface 106 and Rambus channels 202-208 of Welker as disclosing the memory bus. 8/12/02 Office Action at 3. It is noted, however, that it is not the collection of Rambus channels 202-208 that forms the memory bus--more accurately, one Rambus channel is considered one memory bus. *See* Welker, 3:37 ("The Rambus channel is a synchronous high speed *bus* . . . .") (emphasis added).

Welker fails to teach or suggest that a plurality of memory controllers are able to generate memory requests on a memory bus, where at least two of the memory controllers are adapted to generate concurrently pending memory requests on *the* memory bus. As shown in Figure 3 of Welker, only one memory interface control block (MIC) 310 is connected to one Rambus channel. There is no indication that two or more MICs 310 can generate requests on one Rambus channel.

Therefore, claim 1 is allowable over Welker.

With respect to independent claim 10, there is no teaching or suggestion in Welker of a system with a plurality of memory controllers connected to *a* memory bus, with each memory controller to monitor memory requests generated by *another memory controller* in performing memory-related actions. The Office Action pointed to the snoop controller 706 and the snoop cycles generated as teaching the memory controller monitoring memory requests generated by another memory controller. 8/12/02 Office Action at 6. This is incorrect. The snoop controller 706 in the MIC 310 snoops requests from bus masters (not other memory controllers). *See* Welker 8:49-9:49. Note that in claim 10, multiple memory controllers are connected to the *same* memory bus, with one

memory controller to monitor memory requests generated by another memory controller. This is not suggested by Welker.

Therefore, claim 10 is allowable over Welker. Independent claims 15 and 23 are similarly allowable over Welker.

All independent claims are allowable for the reasons set forth above. Dependent claims are allowable for at least the same reasons as corresponding independent claims.

Allowance of all claims is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account No. 50-1673 (9295).

Respectfully submitted,

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VERSION OF CLAIMS INDICATING CHANGES

New claims 24-30 have been added. Amend the claims as indicated below (un-amended claims in smaller font):

1. (Amended) A system comprising:

a memory bus; and

a plurality of memory controllers, each memory controller to generate memory requests on the memory bus according to a predetermined priority scheme,

at least two of the plurality of memory controllers adapted to generate concurrently pending memory requests on the memory bus.

2. The system of claim 1, wherein the predetermined priority scheme comprises a time slot priority scheme.

3. The system of claim 1, wherein the predetermined priority scheme comprises a request-select priority scheme.

4. The system of claim 1, wherein the memory bus comprises a Rambus channel.

5. The system of claim 1, wherein each memory controller generates a memory request during a different predetermined time slot.

6. The system of claim 1, wherein the memory bus comprises plural control portions, each of the control portions associated with corresponding time slot priority schemes.

7. The system of claim 6, wherein the time slot priority schemes are staggered.

8. The system of claim 6, wherein the control portion comprise a row portion and a column portion.

9. The system of claim 1, wherein the memory bus comprises plural portions, each portion associated with a set of memory devices.

10. A system comprising:

a memory bus; and

a plurality of memory controllers connected to the memory bus, each memory controller to monitor memory requests generated by another memory controller in performing memory-related actions.

11. The system of claim 10, wherein the memory-related actions comprise a read-modify-write transaction.

12. The system of claim 10, wherein the memory-related actions comprise a cache coherency action.

13. The system of claim 10, wherein the memory-related actions comprise a memory request.

14. The system of claim 10, the memory controller to determine if the memory bus is available based on outstanding requests from other memory controllers.

15. A method comprising:

providing multiple memory controllers on a memory bus;

generating requests, by the memory controllers, on the memory bus; and

each memory controller monitoring memory-related actions by at least another memory controller.

16. The method of claim 15, wherein generating the requests comprises generating Rambus command packets.

17. The method of claim 15, wherein generating the requests comprises the memory controllers generating the requests one at a time according to a predetermined priority scheme.

18. The method of claim 17, wherein generating the requests comprises generating the requests according to a time slot priority scheme.

19. The method of claim 17, wherein generating the requests comprises generating the requests according to a request-select priority scheme.

20. (Amended) The method of claim 15, further comprising [a]<u>each</u> memory controller determining when to generate a memory request based on the monitoring.

21. (Amended) The method of claim 15, further comprising [a]each memory controller determining if a lock has been asserted due to presence of a read-modify-write transaction.

22. (Amended) The method of claim 15, further comprising [a]each memory controller performing a cache coherency action based on the monitoring.

23. An article comprising one or more storage media containing instructions that when executed cause a memory controller to:

monitor memory requests from another memory controller on a memory bus;

determining if a memory request can be generated on the memory bus based on the monitoring.

24. (New) The system of claim 1, wherein the plurality of memory controllers are connected to the memory bus.

25. (New) The system of claim 1, wherein one of the at least two memory controllers is adapted to generate its memory request on the memory bus before data is returned for the memory request of the other one of the at least two memory controllers.

26. (New) The system of claim 10, wherein at least two of the memory controllers are adapted to generate concurrently pending memory requests on the memory bus.

27. (New) The system of claim 26, wherein one of the at least two memory controllers is adapted to generate its memory request on the memory bus before data is returned for the memory request of the other one of the at least two memory controllers.

28. (New) The method of claim 15, wherein generating the requests on the memory bus comprises at least two of the memory controllers generating concurrently pending requests on the memory bus.

29. (New) The method of claim 28, wherein generating concurrently pending requests comprises one of the at least two memory controllers generating its request before data is returned for the request of the other of the at least two memory controllers.

30. (New) The article of claim 23, wherein the memory controllers are connected to the memory bus.